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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,134	KUSUNOKI, MITSUGU	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06-10-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The modifications to the drawings were received on 06/10/2005. These modifications are accepted by the Examiner.

Specification

The modifications to the specification were received on 06/10/2005. These modifications are accepted by the Examiner.

Claim Objections

In view of the amendment filed on 06/10/2005, the Examiner withdraws claim objections of claims 1-11 of the previous Office Action.

Claim Rejections - 35 USC § 112

In view of the amendment filed on 06/10/2005, the Examiner withdraws the 35 USC § 112 rejections to claims 1-11 of the previous Office Action.

Response to Arguments

Applicant's arguments filed on 06/10/2005 have been fully considered but they are not persuasive.

As per claim 1:

The Applicant contends, "Regarding claim 1, Applicant submits that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of this claim of, inter alia, a semiconductor integrated circuit that includes a first circuit block, a second circuit block, a first signal path, a second signal path, a first buffer circuit and a second buffer circuit where the

circuit blocks, the first and second signal paths, and the first and second buffer circuits are formed on a single semiconductor substrate, or where the clock signal and the data signal are transmitted in parallel to each other on the first and second signal paths, and the data signal is taken by the second circuit block by the clock signal. The Examiner admits that Takahashi et al. does not disclose or suggest details of the clock and data transmission paths between the different blocks as recited in the claims of the present application, but asserts that Isobe et al. discloses these limitations. Specifically the Examiner appears to assert that Isobe et al. discloses a clock signal and a data signal being transmitted in parallel with each other on the first and second signal paths, and the data signal being taken by the second circuit block by the clock signal, in Fig. 13, block 92, 90 and 91, and col. 13, lines 46-47. However, these portions of Isobe et al. merely disclose a block diagram of a data transmission facility to implement full-duplex data transmission using two printed circuit boards 19, 29, and the transmission lines 90-92 between the two printed circuit boards. This is not circuit blocks, first and second signal paths, and first and second buffer circuits being formed on a single semiconductor substrate, as recited in the claims of the present application. Isobe et al. does not disclose or suggest anything related to a semiconductor integrated circuit. Isobe et al. teaches away from the limitations in the claims of the present application in that it discloses two printed circuit boards and transmission lines between the printed circuit boards. This is not circuit blocks and signal paths formed on a single semiconductor substrate. Moreover, this is not a semiconductor integrated circuit wherein a clock signal and a data signal are transmitted in parallel to each other on the

first and second signal paths and the data signal is taken by the second circuit block by the clock signal, as recited in the claims of the present application.

Moreover, the Examiner asserts that Isobe et al. discloses at least a first buffer circuit connected to a first signal path in such a manner as to constitute the first signal path and at least a second buffer circuit connected to the second signal path in such a manner as to constitute the second signal path at Fig. 13, blocks 92- 16-26 and blocks 91-3, and col. 13, lines 62-65. However, as noted previously, these portions of Isobe et al. merely disclose two printed circuit boards and the transmission lines between the two printed circuit boards. This is not a first buffer circuit constituting a first signal path and a second buffer circuit constituting a second signal path, the first and second buffer circuits placed between the first and second circuit blocks and formed on a single semiconductor substrate, as recited in the claims of the present application. These portions of Isobe et al. merely disclose logic gates on one printed circuit board and phase amount adjustment groups on a second separate printed circuit board."

In conclusion Applicant contents that none of the references discloses the claimed invention, specifically the first and second buffer circuits placed between the first and second circuit block, and formed on a single substrate as stated in pages 14-18 in the remarks.

The Examiner disagrees and asserts, that, as indicated in the previous Office Action the references of Isobe and Takahashi shall be consider together, and they are analogous art because they are from similar problem area. In fact these references were sent by the Applicant in a 1449 form. Isobe doesn't teach away because he

doesn't express that his technique can not be use in an integrated circuit. Isobe teaches a method of correcting skew in high speed data transmission and the combination of Takahashi and Isobe teaches that this correction occurs in a single substrate.

The Applicant contends, "Further, Applicants submit that there would be no motivation to combine Takahashi et al., which relates to reducing clock skew on a semiconductor chip, with Isobe et al., which relates to a data transmission apparatus including two circuit boards that "eliminates the need for strict clock skew management . . . " (see, Abstract). These two references present different solutions for a problem in two different environments. Takashi et al. relates to a semiconductor chip, whereas in contrast, Isobe et al. discloses two circuit boards. One of ordinary skill in the art would have no motivation to combine these two references since their techniques are for different environments and are in contrast with each other. Moreover, this combination fails to achieve the limitations in the combination of each of the claims of the present application.".

The Examiner disagrees and asserts, that, as indicated in the previous Office Action the suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe abstract). For these reasons and the reason stated en the previous Office Action, the rejection of claim 1 is maintained.

As per claim 2-11:

The Applicant contends, "Regarding claims 2-11 and new claim 12, Applicant submits that these claims are dependent on independent claim 1 and, therefore, are

patentable at least for the same reasons noted previously regarding this independent claim. For example, Applicant submits that none of the cited references disclose or suggest wherein said second circuit block includes a plurality of circuits operated in synchronism with the internal clock generated based on the clock signal received from said second signal path, and said clock distribution line pattern of said second circuit block is configured to distribute said internal clock to said plurality of circuits through the substantially same length of path', or wherein said second circuit block includes a phase shifting circuit for generating a clock signal out of phase by one half period of the data transmission cycle based on the received clock, and a phase adjusting circuit for generating a clock signal giving a timing of taking data to said holding means based on the clock signal generated by said phase shifting circuit, and wherein said phase adjusting circuit operates to adjust the phase of the clock signal supplied to said holding means in such a manner that the clock signal generated by said phase- shifting circuit is in phase with the phase of the clock signal supplied to said holding means; or wherein said holding means is configured to take said received data signal substantially at the center between the changing points of said received data signal', or wherein the first buffer circuit is placed in a predetermined length of the first signal path, and the second buffer circuit is placed in said predetermined length of the second signal path."

The Examiner disagrees and asserts, that, as indicated in the previous Office Action because the rejection of claim 1 is maintained, the rejections of claims 2-11 are also maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (JP 05159080), and further in view of Isobe et al. (US 6078623).

As per claim 1 Takahashi et al. (JP 05159080) disclose a semiconductor integrated circuit comprising a first circuit block and a second circuit block each having a clock distribution line pattern (figure 1 blocks 10a to 10d paragraph [0008]); where the circuit blocks are formed on a single semiconductor substrate (figure 1 blocks 10a to 10d paragraph [0008]); and where the first and second signal paths have substantially the same wiring conductor length (figure 4 paragraph [0013]). Takahashi et al. (JP 05159080) doesn't disclose the details of the clock and data transmission paths between the different blocks. Isobe et al. (US 6078623) disclose the data and clock transmission paths between two different circuit blocks, with a first signal path for transmitting a data signal from a first circuit block to a second circuit block (figure 13 block 92); a second signal path for transmitting a clock signal from said first circuit block to said second circuit block (figure 13 block 91); and at least a first buffer circuit connected to the first signal path in such a manner as to constitute the first signal path and at least a second buffer circuit connected to the second signal path in such a manner as to constitute the second signal path the first and second buffer circuits placed between the first and second circuit blocks', (figure 13 blocks 92-16-26 and

blocks 91-40 column 13 lines 62-65); where the clock signal and the data signal are transmitted in parallel to each other (figure 13 blocks 90 92 and 91 column 13 line 46-47). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 2 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also disclose an output latch circuit for latching the data signal to be transmitted, the second circuit block has an input latch circuit for latching the data signal to be received, and the output latch circuit and the input latch circuit are configured to perform the latch operation in response to the clock signals before and after, respectively, being transmitted from the first circuit block to the second circuit block (figure 13 blocks 11, 15, 25 and 21 column 14 line 7-9). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The

suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 3 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also disclose a first circuit block that is configured to send the next data signal and the clock signal to the first and second signal paths before arrival of the transmitted data signal clock signal at the second circuit block (figure 13 column 14 line 3-7). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 4 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Takahashi et al. (JP 05159080) also disclose that the second circuit block includes a plurality of circuits operated in synchronism with the internal clock generated based on the clock signal received from the second signal path, and the clock distribution line pattern of the second circuit block is configured to distribute the internal clock to the plurality of circuits through the substantially same length of path (figure 1 blocks 10a to 10d paragraph [0009]). Takahashi et al. (JP 05159080) and

Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 5 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also disclose that the circuit blocks are configured in such a manner that when the data signal is not sent out to the second circuit block from the first circuit block, the clock signal is not sent out from the first circuit block to the second circuit block (figure 13 blocks 11, 15, 25 and 21 column 14 line 7-9). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 6 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Takahashi et al. (JP 05159080) also disclose that a third signal for

feeding back the clock signal received by the second circuit block to the first circuit block is inserted between the first and second circuit blocks, and the first circuit block includes a phase adjusting circuit for adjusting the phase of the clock signal sent out from the first circuit block in such a manner that the clock signal in the first circuit block is in phase with the clock signal fed back (figure 3 paragraph [0011]). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 7 Takahashi et al. (JP 05159080) also disclose that a phase adjusting circuit includes a phase detecting circuit for generating a phase difference signal representing the phase difference obtained by comparing the phase of the clock signal in the first circuit block with the phase of the clock signal fed back, and variable delay circuits with the delay time thereof variable based on the phase difference signal from the phase detecting circuit (figure 3 blocks 31-33 paragraph [0011] and [0012]). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data

transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 8 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Takahashi et al. (JP 05159080) also disclose that the second circuit block includes a plurality of circuits operated in synchronism with a clock signal different from the clock signal received, and the clock distribution line pattern of the second circuit block is configured to distribute different clock signal to a plurality of the circuits through paths having substantially the same length (figure 1 paragraph [0010]). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 9 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also teach that the second circuit block includes means for taking the serial data signal received from the first signal path,

based on the received clock signal and storing the serial data signal for at least two periods of the received clock signal, and means for reading the data signal stored in the storage means by a clock signal different from the received clock signal (figure 14 block 102 and 103, column 14 lines 18-19). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 10 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also teach that the second circuit block includes a phase shifting circuit for generating a clock signal out of phase by one half period of the data transmission cycle based on the received clock, and a phase adjusting circuit for generating a clock signal giving a timing of taking data to the holding means based on the clock signal generated by the phase shifting circuit, and where the phase adjusting circuit operates to adjust the phase of the clock signal supplied to the holding means in such a manner that the clock signal generated by the phase-shifting circuit is in phase with the phase of the clock signal supplied to the holding means (figure 14 blocks 26, 21, 22 25 and 40, column 13 lines 54-62). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are

from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 11 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also teach that the holding means is configured to take the received data signal substantially at the center between the changing points of the received data signal (figure 14 blocks 26, 21, 22 25 and 40, column 14 lines 7-9). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 12 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also teach that the first buffer circuit is placed in a predetermined length of the first signal path, and the second buffer circuit is placed

in said predetermined length of the second signal path (figure 13 blocks 92-26 and blocks 91-40 column 13 lines 62-65). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
06-20-2005

KEVIN BURD
PRIMARY EXAMINER